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Improved Analog Performance in Strained Si MOSFETs using the Thickness of the Silicon Germanium Strain Relaxed Buffer as a Design Parameter

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Abstract- **The impact of self heating in strained Si MOSFETs on the switching characteristics of a CMOS inverter and voltage gain of a push-pull inverting amplifier is assessed by TCAD simulations. Strained Si nMOSFETs on 4 µm and 425 nm thick silicon-germanium strain relaxed buffers (SiGe SRB) are co-fabricated with silicon control nMOSFETs and used to calibrate the TCAD models. Measured data shows a 50% reduction in thermal resistance from 30.5 KmW^{-1} to 16.6 KmW^{-1} as the thickness of the SiGe SRB is scaled from 4 µm to 425 nm. Using the calibrated models, electrothermal simulations of CMOS inverters are performed by accounting for heat generation from carrier flow using the fully coupled energy balance equations for electrons and holes. The results of the TCAD simulations show that the inverter voltage gain can be maximized by balancing the opposing effects of drain induced barrier lowering, which increases the drain conductance and self heating, which reduces the drain conductance. Drain induced barrier lowering is shown to limit the simulated voltage gain of the Si control inverter whereas self-heating in the strained Si nMOSFET on the 4 µm thick SiGe SRB is shown to cause anomalous operation in the simulated inverter characteristics. The inverter voltage transfer characteristics simulated with the strained Si nMOSFETs on the 425 nm SiGe SRB exhibited the highest voltage gain. The thickness of the SiGe SRB is presented as a design parameter for optimizing the analog performance of strained Si MOSFETs.**

Index Terms- **Analog MOSFET, Inverter, Self-heating, Silicon-Germanium, Strained Silicon, Voltage gain, Voltage Transfer Characteristics.**

I. INTRODUCTION

Strained silicon (Si) technology has been identified as source of performance enhancement in complementary metal oxide on semiconductor (CMOS) technology [1]. Improvements in electron mobility have been observed in tensile strained silicon layers due to the lower effective mass and reduced carrier scattering in the conduction band as a result of strain induced band splitting [2]. Tensile strain can be incorporated into the metal oxide on semiconductor field effect transistor (MOSFET) channel by silicon nitride capping layers (uniaxial or local strain) or strained layer hetero-epitaxy (biaxial or global strain). Biaxial strain requires the epitaxial growth of silicon on a silicon-germanium strain relaxed buffer (SiGe SRB), which has been observed to have a lower thermal conductivity than silicon [3]. The lower thermal conductivity of SiGe is due to the reduced phonon mean free path as a result of alloy scattering [4]. When a MOSFET conducts current, carrier collision with the crystal lattice in the channel causes atomic vibrations which are manifested as a rise in the channel temperature. The low thermal conductivity SiGe SRB separates the source of heat generation in the channel from the higher thermal conductivity Si substrate which acts as the heat sink. As a result, heat is accumulated in the strained silicon channel layer which gives rise to increased phonon scattering and negative conductance characteristics at high power densities [5, 6]. Since the drain current and power density is higher in short channel devices, self-heating increases as the channel length is reduced. Short channel devices also have higher thermal resistances because the smaller cross-sectional area constricts heat flow away from the channel [7]. The magnitude of the temperature rise in the strained Si channel layer will increase with the thickness of the SiGe SRB since the efficiency of heat dissipation into the Si substrate will reduce with increasing spacing between the heat source (Si channel) and the heat sink (Si substrate). As a result, thin SiGe SRBs have been identified as a counter-measure to self heating and have demonstrated lower thermal resistances and improved performance enhancements [6, 8-10]. The impact of negative drain conductance ($-g_{DS}$) from self heating and the SiGe SRB thickness on the self gain and the analog design space of strained Si nMOSFETs have been assessed and reported [11]. It was shown that the design space is improved and the occurrence of negative self gain is reduced in strained Si nMOSFETs on thin SiGe SRBs [12].

In this paper, the impact of self heating and SiGe SRB scaling on the simulated characteristics of a CMOS inverter is assessed. The device characteristics of strained Si nMOSFETs on 4 μm and 425 nm thick SiGe SRBs are used to calibrate the technology computer aided design (TCAD) models that are used to simulate the inverter. The fully coupled energy balance equation is used to account for self heating in the model. Since the inverter in an analog circuit is also a push-pull inverting amplifier, the impact of the SiGe SRB thickness and self heating on the voltage gain of the inverting amplifier is assessed. Section II discusses device fabrication and electrical results of the Si control and strained Si nMOSFETs. Section III discusses the TCAD model calibration using the measured data. Section IV discusses the simulation results of the CMOS inverter. Section V concludes the paper.

II. DEVICE FABRICATION AND ELECTRICAL RESULTS

A Si control and two strained Si on SiGe SRB wafers were co-processed. One wafer comprised of a conventional strained Si layer on thick SiGe SRB whereas the other comprised of strained Si on a thin SiGe SRB. The thick SiGe SRB comprised of a 2.5 μm graded buffer, a 1.5 μm constant composition $Si_{0.8}Ge_{0.2}$ layer and a 10 nm tensile strained Si layer. The final germanium (Ge) content of the SiGe buffer was 20%. In the case of the thin SiGe SRB, a layer of SiGe:C was used to achieve strain relaxation. The total thickness in the thin SRB was 425 nm and the Ge content was also 20%. MOSFETs were co-fabricated on the respective wafers through a CMOS process flow. Further details of the MOSFET fabrication process are in [5, 12].

The effective electron mobility was measured on 1 µm (L_G) by 10 µm (W) nMOSFETs using the split CV technique [13]. The results of the measurement are shown in Fig. 1 where 100% mobility enhancement is observed in the strained Si nMOSFETs compared with the Si control device. The drain conductances (g_{DS}) of 100 nm gate length MOSFETs are measured using an impedance analyzer with a 10 MHz signal at the drain while biasing the gate. The measurement set-up can be used to extract the thermal resistance (R_{TH}) of the MOSFET by comparing the high frequency and DC g_{DS}. Applying a high frequency drain-source signal suppresses the effect of self heating, hence the intrinsic performance of the MOSFET can be measured. Details of the experimental set up are in the literature [5, 14-16]. The measured g_{DS} is integrated with respect to the drain voltage (V_{DS}) so as to extract the output characteristics. The resulting output characteristics of the 100 nm gate length nMOSFETs are shown in Fig. 2, where the drain currents (I_{DS}) are shown as functions of V_{DS} at 10 MHz and DC. It can be seen in Fig. 2 that the strained Si nMOSFETs exhibit the negative g_{DS} characteristic at high V_{DS} due to self heating at DC. This negative g_{DS} characteristic is more severe in the strained Si nMOSFET on the thick SiGe SRB. Fig. 2 also shows that the negative g_{DS} characteristic disappears at 10 MHz and the I_{DS} enhancement compared with the Si control is restored. A semi-empirical MOSFET model is used to calculate the temperature rise in the MOSFET channel by comparing the g_{DS} at 10 MHz and DC [5, 14-16]. The R_{TH} is then calculated by dividing the temperature rise by the DC power, which is calculated as $I_{DS}.V_{DS}$. The R_{TH} extracted on the strained Si nMOSFET on the thick and thin SiGe SRB was calculated as 30.5 $K.mW^{-1}$ and 16.6 $K.mW^{-1}$ respectively which indicates a 50% improvement in the strained Si nMOSFET on the thin SiGe SRB. In the work of Su et al [17], a model was developed for estimating the R_{TH} of an SOI MOSFET which showed that the R_{TH} is proportional to the square-root of the buried oxide thickness. This model was subsequently applied to strained Si MOSFETs on SiGe SRBs in the work of Jenkin et al [18] and Agaiby et al [5]. Hence, by reducing the SRB thickness from 4 μm to 425 nm, the R_{TH} is expected to reduce by 67% whereas experimental measurements here show a reduction by 50%. This variation between the calculated and measured R_{TH} percentage improvement in the thin SRB is due to the fact that R_{TH} is determined not only by the SRB thickness but also by other parameters like phonon scattering from the Si/SiGe heterointerface, defects from strain relaxation in the virtual substrate as well as thermal boundary conditions around the channel (oxide interface, source/drain metal contacts, length of the Si_3N_4 sidewall spacer). In the work of Jenkin et al [18], the R_{TH} extracted for a 100 nm gate length strained Si nMOSFET on a 1.5 μm $Si_{0.85}Ge_{0.15}$ SRB with a 15 nm strained Si channel layer was 13.4 $K.mW^{-1}$. In the work of Olsen et al [11], a R_{TH} of 18.9 $K.mW^{-1}$ and 4.5 $K.mW^{-1}$was extracted from 0.4 μm gate length strained Si nMOSFETs fabricated on 2 μm and 200 nm $Si_{0.8}Ge_{0.2}$ SRBs respectively with strained Si channel layers of 15 nm. The R_{TH} values calculated here are comparable to what has been published in literature for strained Si MOSFETs on SiGe SRBs [11, 18].

The self gain (A_V) of the MOSFETs were calculated and shown as functions of V_{DS} in Fig. 3. The discontinuity in the A_V characteristic of the strained Si nMOSFET on the thick SiGe SRB in Fig. 3 is due to the change in polarity of the g_{DS}, as it crosses to zero mark, due to self heating. That this discontinuity in the A_V vs. V_{DS} characteristics does not occur in the strained Si nMOSFET on the thin SiGe SRB is indicative of the fact that self heating is reduced with buffer scaling. The equation of the MOSFET self gain taking self heating into account can be expressed as [12, 19]

$$A_V = \frac{g_{mN}}{g_{DSN} + R_{TH}\theta I_{DSN}} \qquad (1)$$

where g_{mN} is the transconductance, g_{DSN} is the drain conductance, I_{DSN} is the drain current and θ is the temperature sensitivity of the mobility. The discontinuity in the A_V characteristic of Fig. 3 occurs when the denominator in (1) is equal to zero.

It can be seen from the DC output characteristics in Fig. 2 that drain induced barrier lowering (DIBL) is highest in the Si control device where a positive g_{DS} is observable at high V_{DS} i.e. I_{DS} does not fully saturate. DIBL can be calculated by measuring the change in the threshold voltage, V_{TH} as V_{DS} is increased. The gate transfer characteristics (I_{DS} vs. V_{GS}) for the 100 nm gate length Si control, strained Si nMOSFET on the thick and thin SiGe SRB are shown in Fig. 4(a), Fig. 4(b) and Fig. 4(c) respectively. The V_{GS} spacing between the low V_{DS} and high V_{DS} gate transfer characteristics in Fig. 4 is indicative of the extent of DIBL. DIBL is calculated to be 110 mV/V for the 100 nm Si control nMOSFET whereas it is approximately 10 mV/V for the strained Si nMOSFETs on the thin and thick SiGe SRB. Self heating reduces the effect of DIBL in the strained Si devices since its impact on g_{DS} is opposite to that of DIBL.

III. TCAD MODEL

Electrothermal modeling of MOSFETs is traditionally done by solving the electron-hole drift-diffusion equations coupled with the heat flow equation. In the *J.E* approach, the heat generated from current flow is calculated by taking the dot product of the electric field, *E*, and current density, *J* (*J.E*) [7]. The total heat generated in the MOSFET is the sum of the heat generated from Joule heating and that from non-radiative electron-hole generation and recombination processes [20]. It is assumed that the peak of heat generation coincides with the position of the maximum electric field. However, as devices are scaled to the order of magnitude of the electron mean free path, quasi-ballistic and non-local effects become important. If the electrical carriers transit from the source to the drain before undergoing enough inelastic collisions to dissipate heat into the lattice, i.e. if there is insufficient time to thermalize, the *J.E* approach becomes less accurate since it assumes that the carriers are in thermal equilibrium with the lattice. Non-local effects occur because carriers thermalize at distances several mean free paths away from the electric field peak, hence, in nanometer scale length devices, the peak of the electric field does not coincide with the temperature peak. Furthermore, the Fourier heat diffusion law cannot accurately model heat flow at time scales on the order of magnitude of the phonon relaxation time [20]. Due to the limitations of the drift-diffusion approach for nanometer scale MOSFETs, heat conduction is most accurately simulated by solving the Boltzmann transport equation for phonons [21]. These advanced simulation techniques are required for modeling nanoscale hot-electron effects, temperature sensitive breakdown effects, impact ionization in nanoscale devices, device hot-spots and carrier velocity overshoot. Since the purpose of this study is limited to understanding the impact of self heating and $-g_{DS}$ on the circuit performance of 100 nm gate length strained Si MOSFETs, the commercial device simulation software from Synopsys, MEDICI, is sufficient. The "lattice temperature advanced application" module in MEDICI was invoked to simulate self heating. To account for non-local effects, the hydrodynamic carrier transport model is used to decouple the lattice temperature from the carrier temperature. The hydrodynamic model involves solving the energy balance equations coupled with the Poisson equation and the electron/hole continuity equations.

The strained Si MOSFETs are simulated in MEDICI by incorporating the values of the extracted and measured experimental parameters into the model. An average low field mobility of 250 $cm^2V^{-1}S^{-1}$ was programmed into the simulation code for the strained Si nMOSFETs whereas 125 $cm^2V^{-1}S^{-1}$ was programmed for the Si control. The source-drain resistance (R_{SD}) of the MOSFETs is measured using the "shift and ratio" method [22] and the extracted value is incorporated into the MEDICI model as a contact resistance in the electrode statement. An effective channel length of 85 nm, also extracted from the "shift and ratio" method, was incorporated into the MEDICI model by extending the source/drain regions into the channel. The effective substrate doping is calculated from capacitance-voltage measurements [23] and incorporated into the MEDICI model. Table 1 shows lists the parameters measured or calculated and used in the MEDICI model. The thickness of the strained silicon channel layer is defined as 10 nm in the mesh and the substrate terminal is defined as the thermal heat sink and set to 300 K. A lumped R_{TH} element is defined and connected to the 300 K heat sink as the thermal boundary condition. Setting appropriate and realistic thermal boundary conditions for the source, drain and gate terminals are important because it affects the temperatures calculated. Setting no thermal boundary conditions assumes adiabatic conditions in the MOSFET and hence represents the worst-case scenario of self heating since no heat flows out of the device. However the lumped R_{TH} element connected to the substrate will approximate the combined thermal boundary conditions for all the terminals. The R_{TH} is used as the variable for matching the measured data with the simulated data. It is expected to be higher for the strained Si nMOSFET on the thick SiGe SRB because higher R_{TH} values have been extracted experimentally.

IV. RESULTS AND DISCUSSION

Fig. 5(a) shows the output characteristics simulated in MEDICI together with the measured output characteristics where it can be seen that there is a good match for V_{GS}-V_{TH}=0.5 V, 1 V, 1.5 V and 2 V. A lumped R_{TH} of 1.4 x 10^5 Kμm/W and 1 x 10^5 Kμm/W was required to match the simulated and output characteristics of the strained Si nMOSFET on the thick and thin SiGe SRB respectively. This translates to 14 KmW^{-1} and 10 KmW^{-1} for a 10 μm gate width device which deviates from the measured R_{TH} on the strained Si nMOSFET on the thick and thin SiGe SRB by 50% and 40% respectively. The R_{TH} determined by the simulations are smaller than those measured experimentally because the simulations assume no heat dissipation through the source, gate and drain terminals. Hence, for the simulator to match the measured output characteristics, a substrate with a lower R_{TH} is required. Fig. 5(b) shows the measured and simulated output characteristics for the strained Si nMOSFETs and the Si control device at V_{GS}-V_{TH}=1.5 V where good matching can be observed.

The MOSFET models were used in the "circuit analysis advanced application" module in MEDICI where the terminals were connected in an inverter configuration. Since the mechanism of heat generation is similar for holes and electrons and the low thermal conductivity SiGe buffer is common to both devices, self heating also occurs in strained Si pMOSFETs on SiGe SRBs [24, 25]. The pMOSFETs in the simulated inverter were not calibrated by measured data hence, the same self heating parameters defined for the nMOSFETs were used. Assuming the same R_{TH} for the nMOSFET and pMOSFET is reasonable since both devices will typically be fabricated on the same wafer. It was reported in the work of Rim et al [26] that hole mobility in tensile strained Si is slightly degraded compared with the Si control for low strain magnitudes and that high strain magnitudes are required for hole mobility enhancement. The impact of low hole mobility on the output characteristics of the CMOS inverter will be to cause asymmetry in the switching characteristics by reducing the switching voltage. For symmetrical inverter operation, the gate width of the pMOSFET used in the inverter simulations was set to 2.5 times that of the nMOSFET to compensate for lower carrier mobility. The voltage transfer characteristic (VTC) of the CMOS inverter can provide useful information on the voltage gain when the inverter is used as a push-pull inverting amplifier. The equation for voltage gain of the push-pull inverting amplifier can be modified by taking self heating into account [19]. The voltage gain equation can be expressed as

$$A_V = -\frac{g_{mN} + g_{mP}}{g_{DSN} + g_{DSP} - \left(R_{TH}\left|\theta_N\right|I_{DSN} + R_{TH}\left|\theta_P\right|I_{DSP}\right)} \qquad (2)$$

where g_{mP} is the transconductance of the pMOSFET, g_{DSP} is the output (drain) conductance of the pMOSFET, θ_N is the temperature sensitivity of the electron mobility, θ_P is the temperature sensitivity of the hole mobility and I_{DSP} is the pMOSFET drain current. The terms in the parenthesis in (2) account for self heating hence, setting R_{TH} to zero reduces (2) to the recognizable equation for the voltage gain of the CMOS inverting amplifier. The negative sign in (2) indicates that the amplifier inverts the input signal i.e. introduces a phase shift of 180˚ [16]. If the self heating terms in the parenthesis become larger than the sum of the drain conductances, then the negative sign becomes positive thereby causing anomalous operation. It was reported in the work of Fox et al [19] that self heating causes non-linear phase shifts and anomalous behavior in CMOS analog amplifiers.

The VTC of the CMOS inverters were simulated for the Si control and strained Si devices with a power supply (V_{DD}) of 2 V. The schematic of the inverter is shown in Fig. 6(a) with the terminal voltages and currents labeled. In Fig. 6(a), V_{GSN} is the gate-source voltage of the nMOSFET, V_{GSP} is the gate-source voltage of the pMOSFET, V_{DSN} is the drain source voltage for the nMOSFET, V_{DSP} is the drain source voltage for the pMOSFET, V_{THN} is the threshold voltage for the nMOSFET, V_{THP} is the threshold voltage of the pMOSFET and I_{DSP} is the drain source voltage of the pMOSFET. Fig. 6(b) shows the full VTC of the simulated CMOS inverters for the Si control and the strained Si nMOSFET on the thin SiGe SRB and partial results for the thick SiGe SRB. The simulation for the case of the thick SiGe SRB could not converge beyond an input voltage of 0.8 V for reasons soon to be discussed. The switching voltage, V_S, is defined as the point on the VTC where the input voltage, V_{IN} is equal to the output voltage V_{OUT} and is labeled in Fig. 6(b) as the intersection point between the VTC and a 45° line from the graph origin. For a perfectly symmetrical inverter with identical nMOS and pMOS characteristics, the inverter switches at $V_S=V_{DD}/2$. In the case of an inverter with a relatively poorer pMOS performance (compared to nMOS) due to lower hole mobility in tensile strained Si (compared to electron mobility), the V_S will be less than $V_{DD}/2$ .i.e. the VTC is shifted leftwards. It can be observed in Fig. 6(b) that the switching characteristic of the inverter with the thin SiGe SRB MOSFET is the most ideal because it has the highest switching slope. The voltage gain of the inverter is calculated by differentiating V_{OUT} with respect to V_{IN} and is shown as a function of V_{IN} in Fig. 7. The voltage gain of the inverter simulated with the thin SiGe SRB MOSFET parameters is 300% higher than that of the Si control. As in Fig. 6(b), the results of the thick SiGe SRB in Fig. 7 are inconclusive due to the inability of the simulator to converge. The impact of self heating on the output characteristics of the MOSFET is to reduce the g_{DS}, whereas other short channel effects like drain induced barrier lowering (DIBL) increase g_{DS}. DIBL causes a positive g_{DS} slope in I_{DS}-V_{DS} saturation characteristics whereas self heating causes a negative g_{DS} slope. Hence, balancing the opposing effects of DIBL and self heating is key for optimal analog operation. For maximum gain amplification, the g_{DS} should be as little as possible especially for short channel devices where high DIBL degrades the voltage gain [27]. The switching slope and voltage gain of CMOS inverters reduces as subthreshold conduction from DIBL increases. The interplay between DIBL and self heating is responsible for the different voltage transfer characteristics shown in Fig. 6(b).

Fig. 8 shows how the VTCs are derived from the output characteristics of the respective devices. V_{OUT} is the intersection point between the nMOSFET and pMOSFET drain currents ($I_{DSN}=I_{DSP}$) for the same V_{IN}. Since the drains of the MOSFETs are connected, there can be only 1 solution for V_{OUT} for any V_{IN}. When V_{IN} is zero, the nMOSFET is off ($V_{GSN}=0\ V$ and $V_{DSN}=V_{DD}$) and the pMOSFET is in the linear mode ($V_{GSP}=-V_{DD}$ and $V_{DSP}=0\ V$). Since the pMOSFET is conducting, V_{OUT} is equal to V_{DD} and this is labeled in Fig. 8(a), 8(b) and 8(c) for the Si control, strained Si on thick SiGe SRB and strained Si on thin SiGe SRB respectively. As V_{IN} increases towards V_S, the nMOSFET goes into saturation ($V_{GSN} - V_{THN} < V_{DSN}$) while the pMOSFET remains in the linear mode ($V_{GSP} - V_{THP} > V_{DSP}$). This part of the VTC is labeled as V_{OUT1} in Fig. 8(a), 8(b) and 8(c). The V_{IN} at which the nMOSFET goes into saturation is a function of V_{THN}, which is strongly dependent on DIBL for short channel devices. As shown in Fig. 4, DIBL is higher in the Si control nMOSFET due to the absence of self heating hence the Si control inverter VTC shows "early switching" as labeled in Fig. 6(b). Because DIBL is low in the strained Si nMOSFETs, there is no early switching in the VTC shown in Fig. 6. In this case, self heating is an advantage for the strained Si nMOSFETs on the thin SiGe SRB. The inverter switches state ($V_{IN}=V_S$) when both MOSFETs go into saturation, which is labeled as V_{OUT2} in Fig. 8(a), 8(b) and 8(c). In the case of the inverter VTC of the strained Si on thick SiGe SRB, (Fig. 8(b)), there is more than one intersection point between I_{DSN} and I_{DSP}, hence there is more than one solution for V_{OUT}. These multiple intersection points are due to the $-g_{DS}$ characteristics in Fig. 8(b) and are the reasons why the simulator is unable to converge to a solution for V_{OUT} in the thick SiGe SRB VTC as shown in Fig. 6(b). This anomalous behavior due to self heating has previously been reported in analog silicon-on-insulator (SOI) circuits where non linear behavior was observed in the output characteristics of inverters and CMOS amplifiers [19]. The output characteristics of the strained Si nMOSFET on the thin SiGe SRB (Fig. 8(c)) do not show multiple intersection points and hence the simulator can converge to a solution for V_{OUT} since there is only one intersection point between I_{DSN} and I_{DSP}. As V_{IN} is increased beyond V_S, the nMOSFET goes into the linear mode ($V_{GSN} - V_{THN} > V_{DSN}$) while the pMOSFET goes into saturation (V_{GSP} - V_{THP} < V_{DSP}). This is labeled as V_{OUT3} in the respective characteristics of Fig. 8. Finally, V_{OUT} reduces to zero as V_{IN} reaches V_{DD}.

The inverter VTC of the strained Si nMOSFET on the thin SiGe SRB exhibits the highest voltage gain and best switching characteristics because DIBL is cancelled out by self heating. DIBL degrades the VTC of the Si control whereas self heating degrades the VTC of the thick SRB. Since both self heating and DIBL reduce as the gate length is increased, this mutual cancellation becomes less critical for longer channel MOSFETs. It is hard to predict which effect will dominate at a specific gate length since DIBL depends on halo implants, channel implants, oxide thickness, junction depth, effective channel length, dopant out-diffusion etc. On the other hand, self-heating depends on the Ge composition, layer thicknesses, physical dimensions, thermal boundaries, material quality etc. Although DIBL and self heating are individually detrimental to the output characteristics of short channel MOSFETs, careful design of strained Si MOSFETs on SiGe SRBs can yield optimum analog performance if the effects are mutually cancelled out.

V. CONCLUSIONS

TCAD models have been calibrated by measured data, used to simulate the voltage transfer characteristics of CMOS inverters and calculate the voltage gain of push-pull inverting amplifiers. Measured data and simulation results show that the thermal resistance is reduced by approximately 50% when the thickness of the SiGe SRB is reduced from 4 μm to 425 nm. The voltage gain of the inverter simulated for the strained Si nMOSFET on the thin SiGe SRB exhibits 300% enhancement compared with the Si control inverter. This significant enhancement in the voltage gain is due to the high output resistance arising from the mutual cancellation between self heating and DIBL. As the input voltage of the inverter reaches the switching voltage, the negative drain conductance characteristics from self heating in the strained Si nMOSFET on the thick SiGe SRB cause multiple solutions for the inverter output voltage, hence the simulator is unable to converge. The case is due to multiple intersection points between the drain currents due to negative conductance. This anomalous behavior is in agreement with what has previously been reported in literature for analog SOI circuits. In the case of the Si control CMOS inverter, the voltage gain is limited by DIBL, which manifests itself in the voltage transfer characteristics as early switching. Although self heating and DIBL are individually deleterious to the analog performance of MOSFETs, balancing their effects for maximizing voltage gain can yield positive results. The thickness of the SiGe SRB can therefore be used to control DIBL and optimize the voltage gain.

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TABLE. 1. MOSFET PARAMETERS USED TO CALIBRATE MEDICI MODELS

Parameter	Thick SRB	Thin SRB	Units	Extraction method
Gate length, L_G	100	100	nm	Defined on mask
Effective channel length, L_{EFF}	85	85	nm	Shift & Ratio
Oxide thickness, t_{OX}	1.4	1.4	nm	CV measurements
Contact resistance, R_{CO}	180	180	Ω-μm	Shift & Ratio
Substrate doping, N_A	1.2	1.2	x 10^{18}cm^{-3}	CV measurements
Effective mobility, μ_{EFF}	250	250	cm^{2}V^{-1}S^{-1}	split CV measurements
Strained Si thickness, t_{Si}	10	10	nm	Taken from TEM
Lumped thermal resistance, R_{TH}	14	10	K.mW^{-1}	Used for fitting

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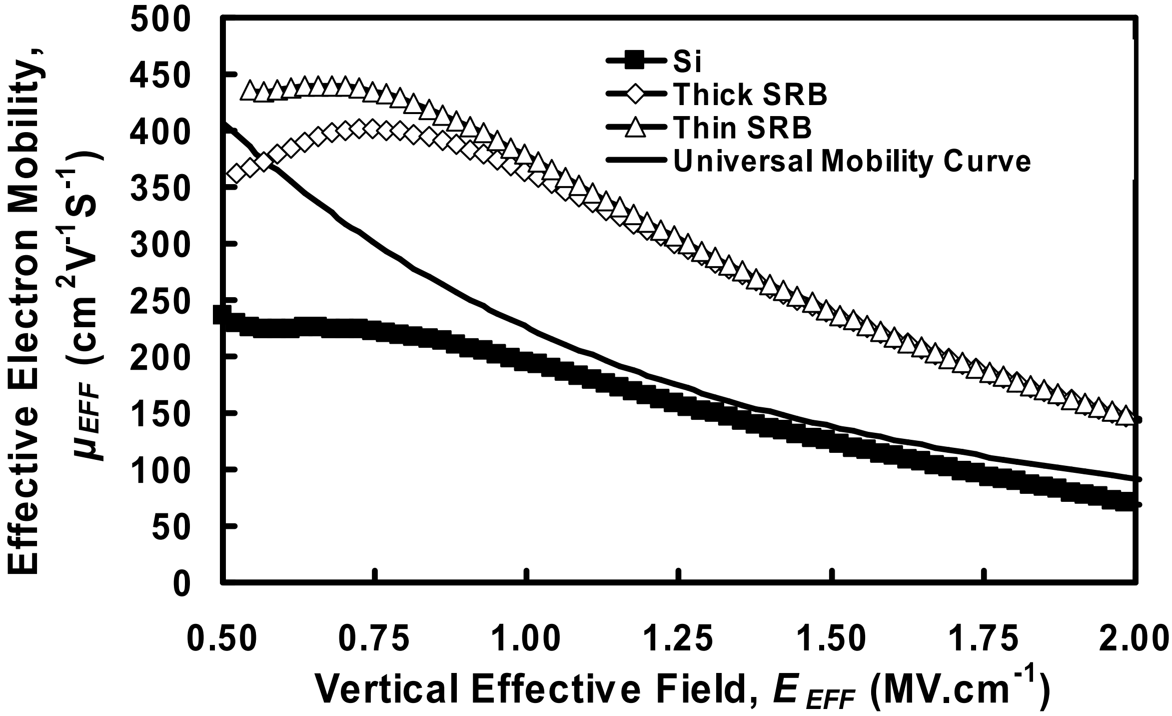

Fig. 1. The effective electron mobility as a function of the vertical effective field for the Si control and strained Si devices on the thin and thick SiGe SRBs. There is 100% mobility enhancement in the strained Si devices compared with the Si control.

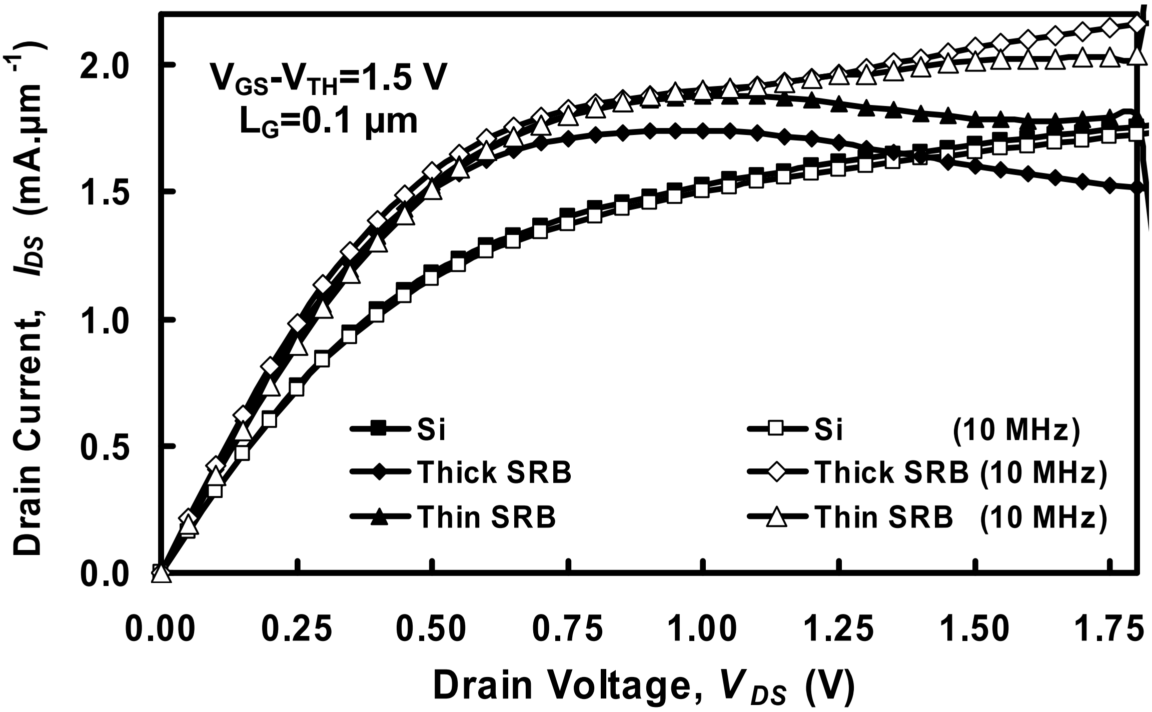

Fig. 2. I_{DS} vs. V_{DS} characteristics with and without self heating effects on 0.1 µm gate length MOSFETs at a gate overdrive V_{GS}-V_{TH} of 1.5 V.

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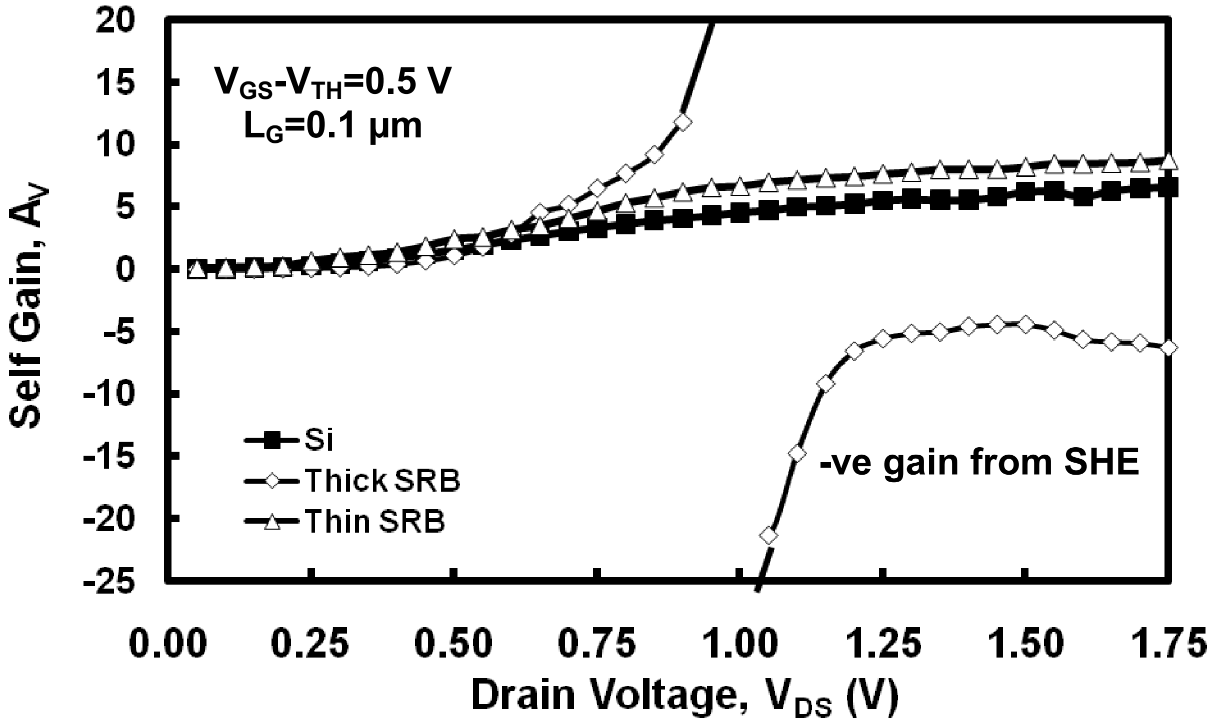

Fig. 3. A_V vs. V_{DS} characteristics for the 100 nm gate length strained Si and bulk Si MOSFETs measured at V_{GS}-V_{TH}=$500\ mV$. Negative g_{DS} due to self heating effects (SHE) causes negative self-gain for the thick SiGe SRB devices at high V_{DS}. This problem is eliminated by the thin SRBs.

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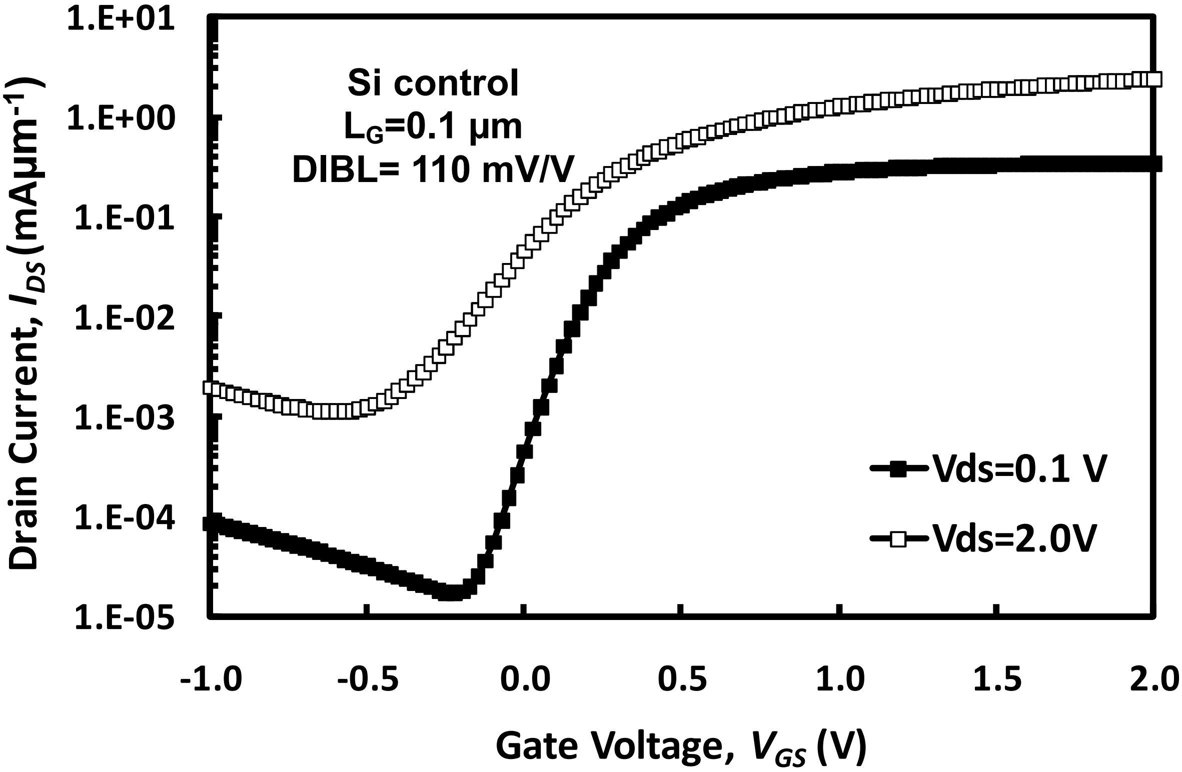

Fig. 4(a). I_{DS} vs. V_{GS} characteristics for the 100 nm gate length silicon control nMOSFET. DIBL is calculated to be 110 mV/V. The separation between the 2 drain current curves shows the impact of DIBL.

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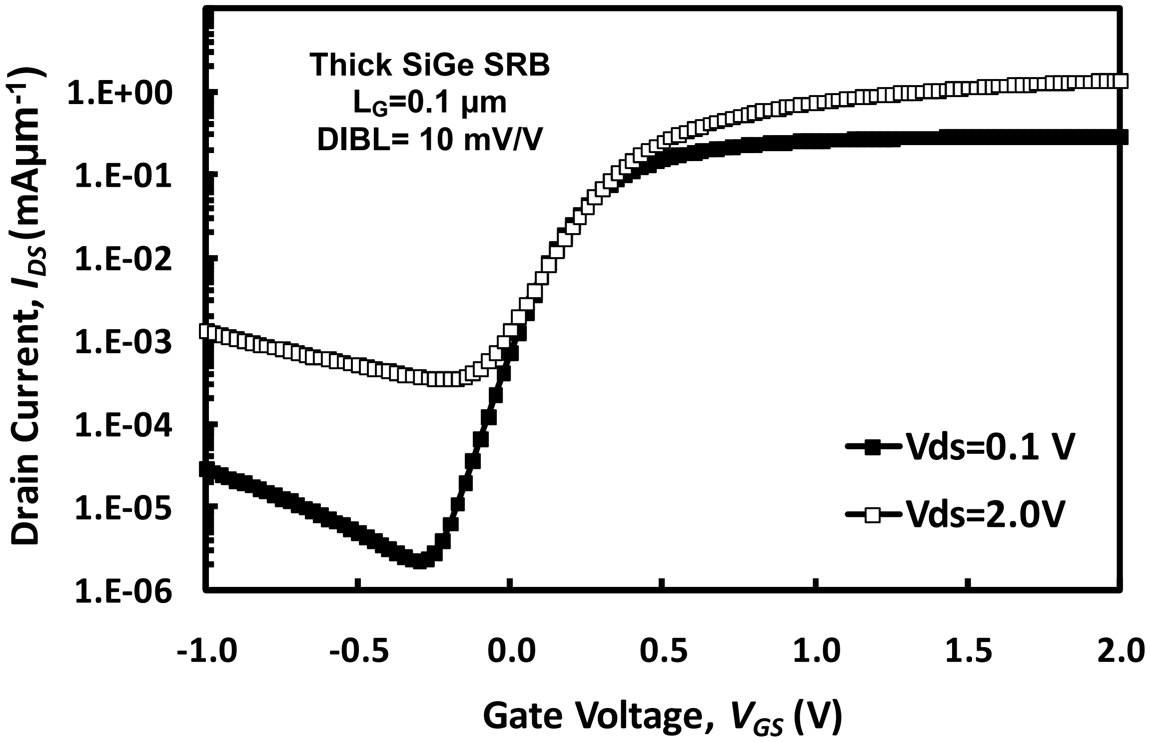

Fig. 4(b). I_{DS} vs. V_{GS} characteristics for the 100 nm gate length strained Si nMOSFET on the thick SiGe SRB. DIBL is calculated to be 10 mV/V. The smaller separation between the drain current characteristics shows that the effect of DIBL is minimal.

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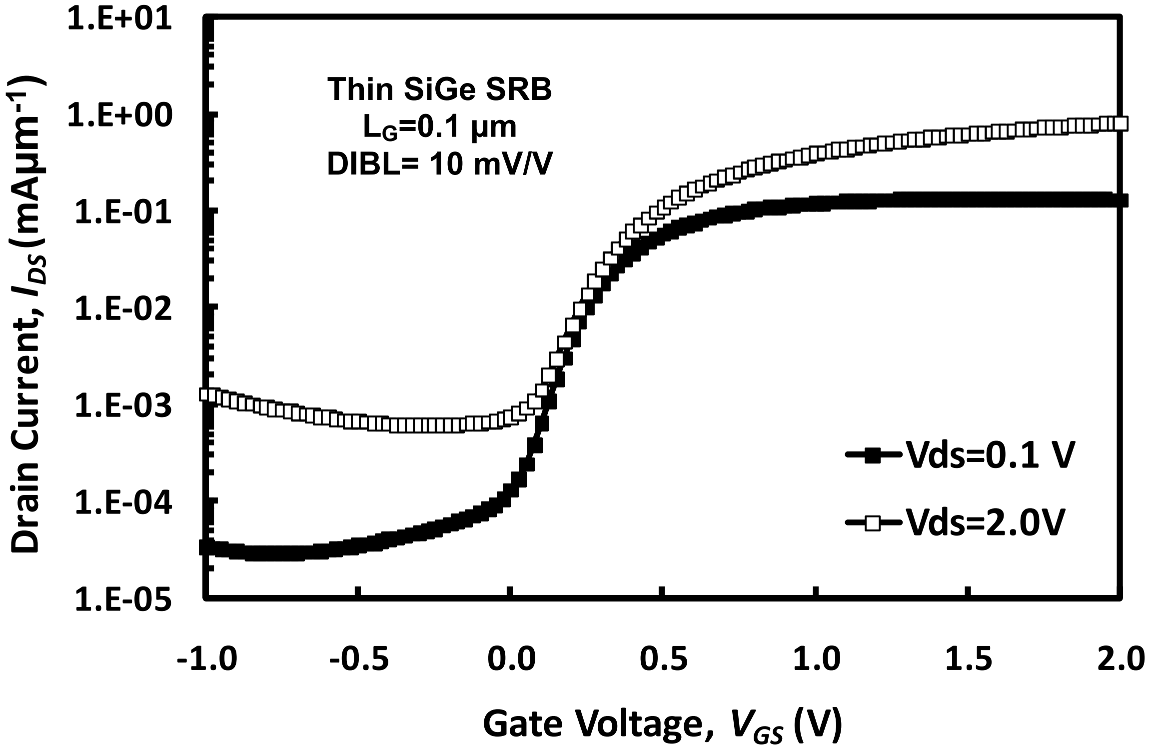

Fig. 4(c). I_{DS} vs. V_{GS} characteristics for the 100 nm gate length strained Si nMOSFET on the thin SiGe SRB. DIBL is calculated to be 10 mV/V. The smaller separation between the drain current characteristics shows that the effect of |DIBL is minimal.

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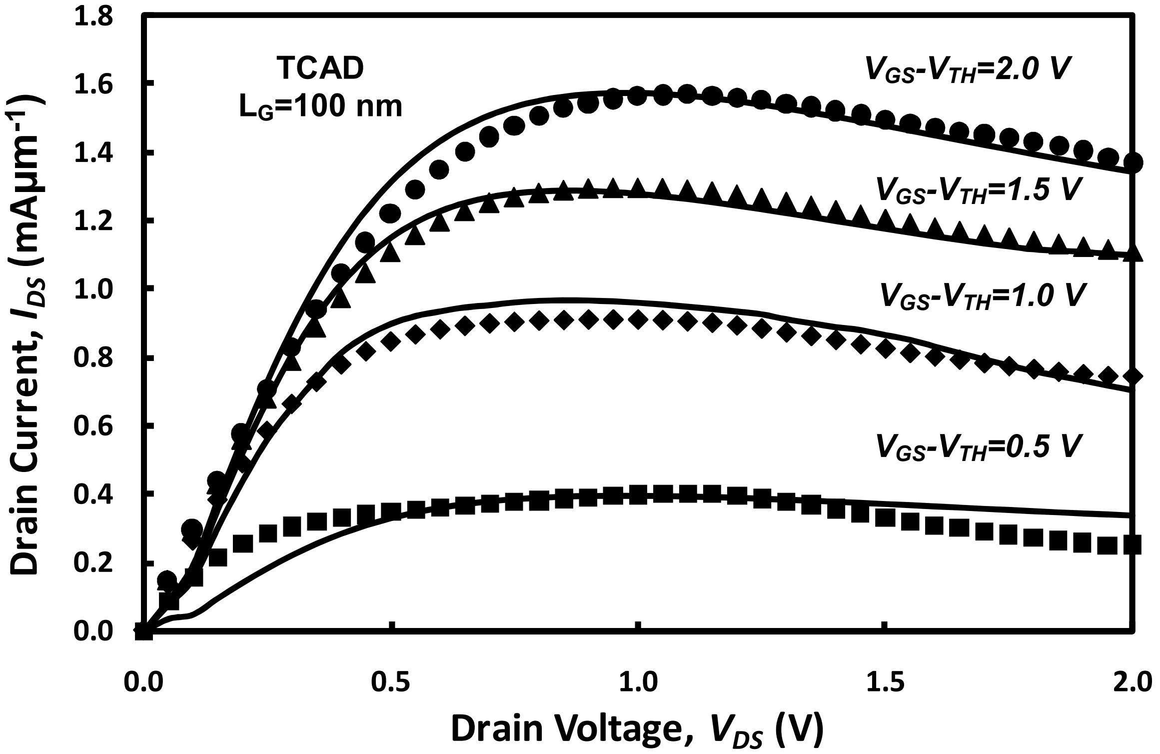

Fig. 5(a). The simulated and measured output characteristics of the 100 nm gate length strained Si nMOSFET on the thick SiGe SRB. The results show good matching between the measured and simulated data.

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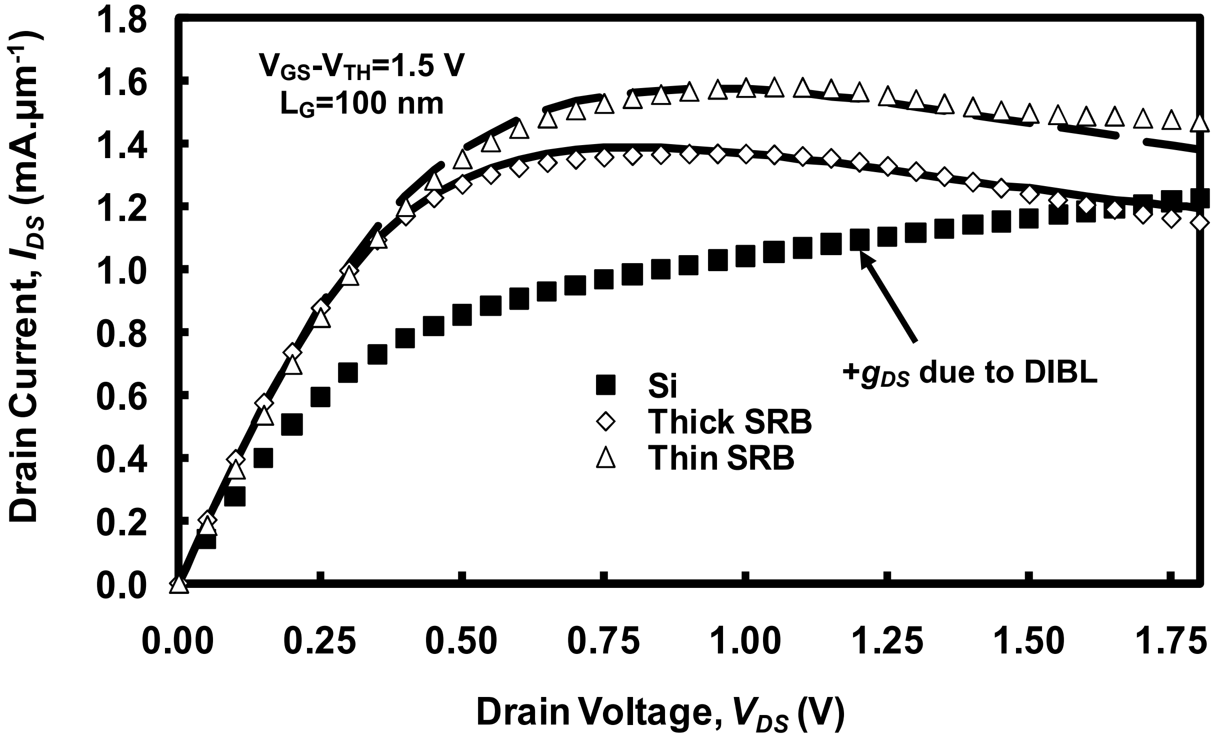

Fig. 5(b). Simulated and measured output characteristics of the 100 nm gate length Si control and strained Si nMOSFETs on the thick and thin SiGe SRBs. A lumped R_{TH} of 1.4 x 10^5 Kμm/W and 1.0 x 10^5 Kμm/W was required to match the simulated output characteristics of the strained Si nMOSFET on the thick and thin SiGe SRB respectively.

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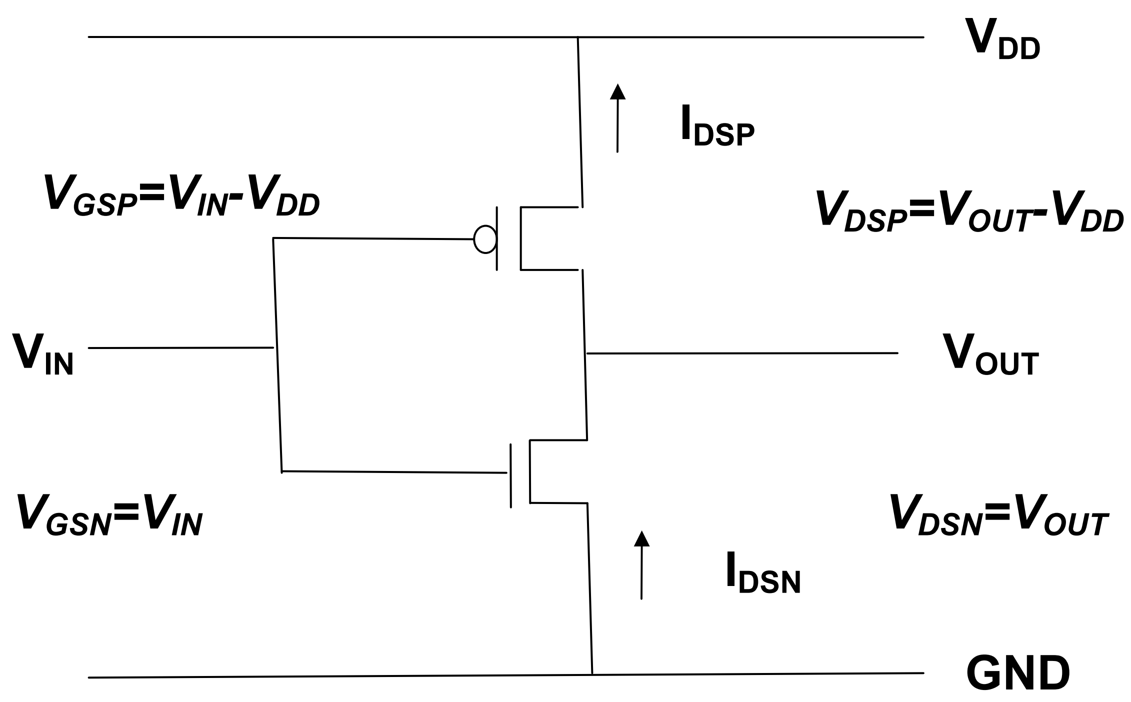

Fig. 6(a). The schematic of the CMOS inverter with the currents and voltages labeled.

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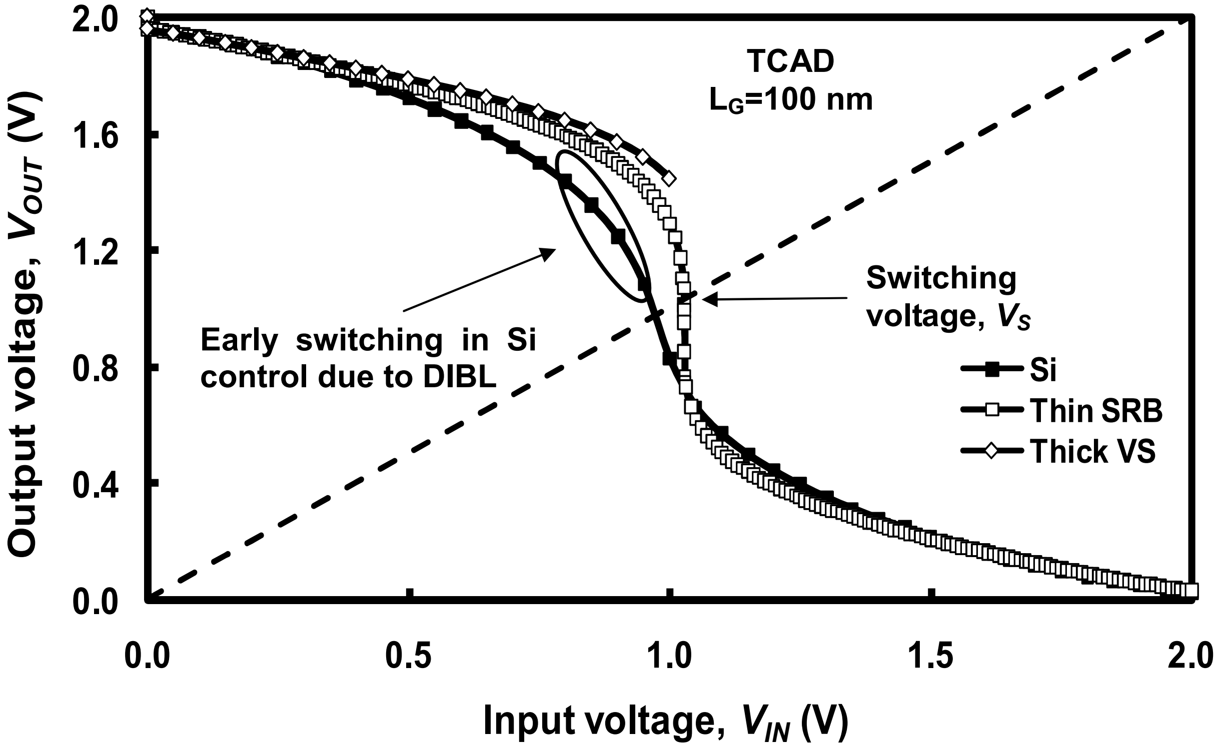

Fig. 6(b). The simulated voltage transfer characteristics of CMOS inverters for Si control and strained Si nMOSFETs on thin and thick SiGe SRBs. Early switching due to DIBL is evident in the VTC of the Si control inverter. The simulator is unable to converge for the VTC of the strained Si nMOSFET on the thick SiGe SRB due to non-linear operation from self heating.

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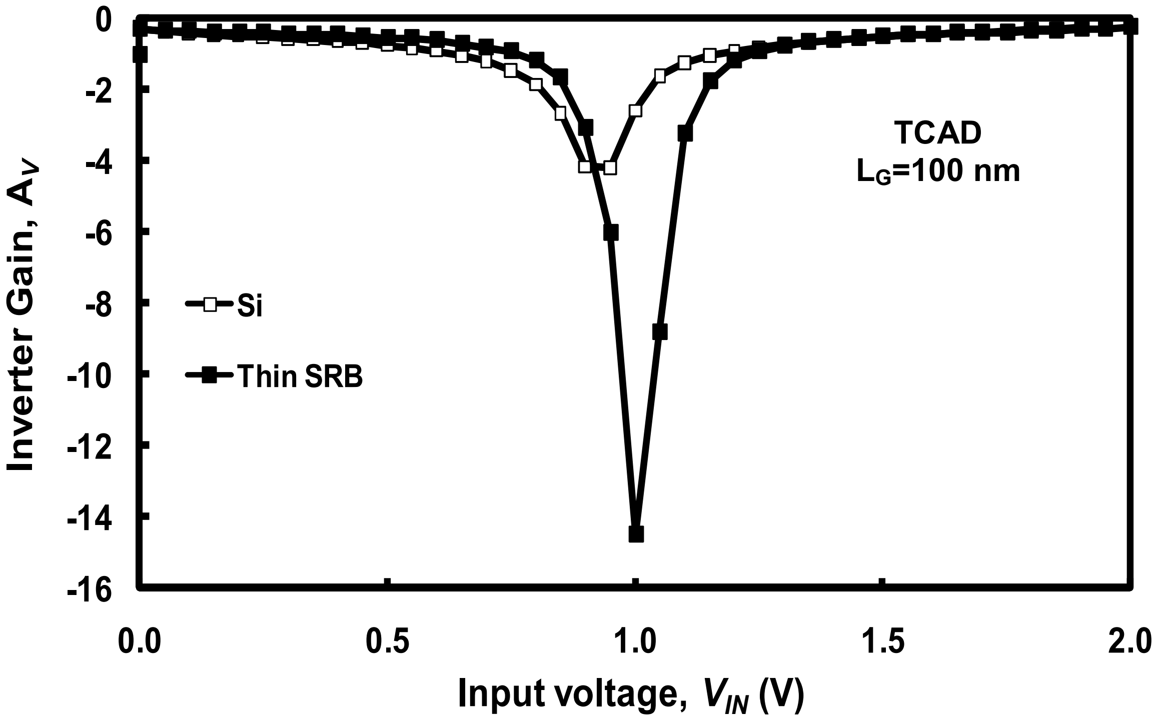

Fig. 7. The voltage gain of the push-pull inverting amplifier as a function of the input voltage for the Si control and strained Si on thin SiGe SRB inverters. There is 300% enhancement in the voltage gain of the strained Si inverter compared with the Si control due to better switching characteristics.

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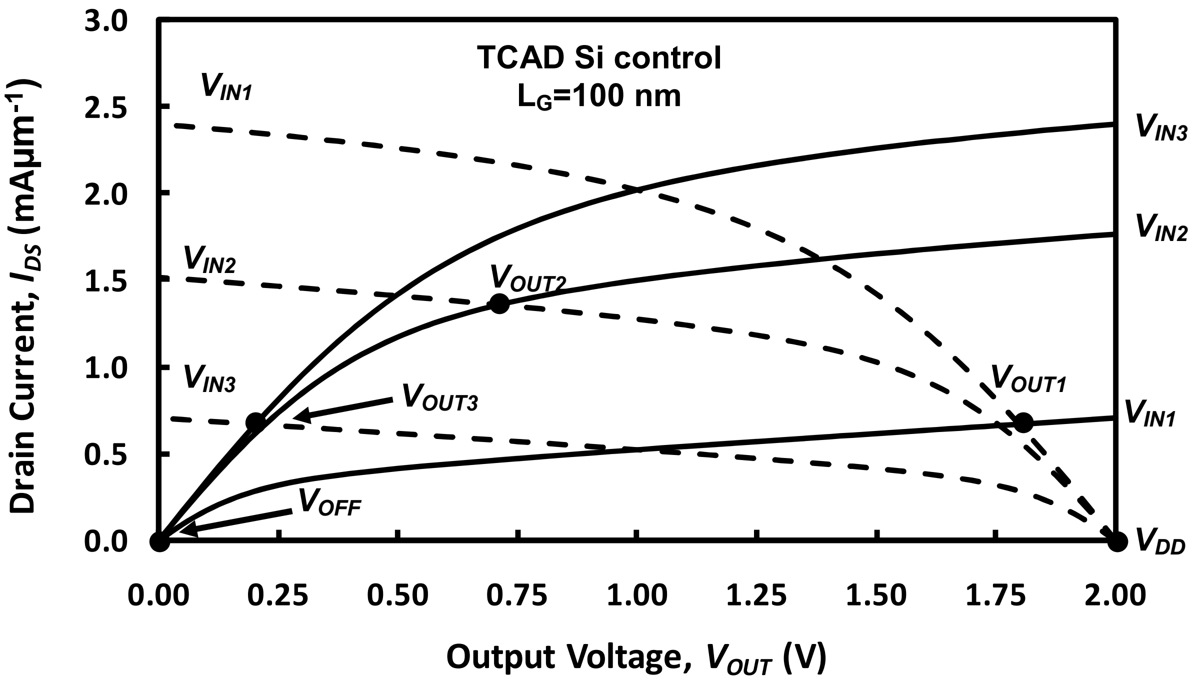

Fig. 8(a). The simulated I_{DS} vs. V_{DS} characteristics of the inverter nMOSFET and pMOSFET using models calibrated with the Si control nMOSFET parameters. The points of intersection between I_{DSN} and I_{DSP} for V_{IN1}, V_{IN2} and V_{IN3} are used to determine V_{OUT1}, V_{OUT2} and V_{OUT3} respectively.

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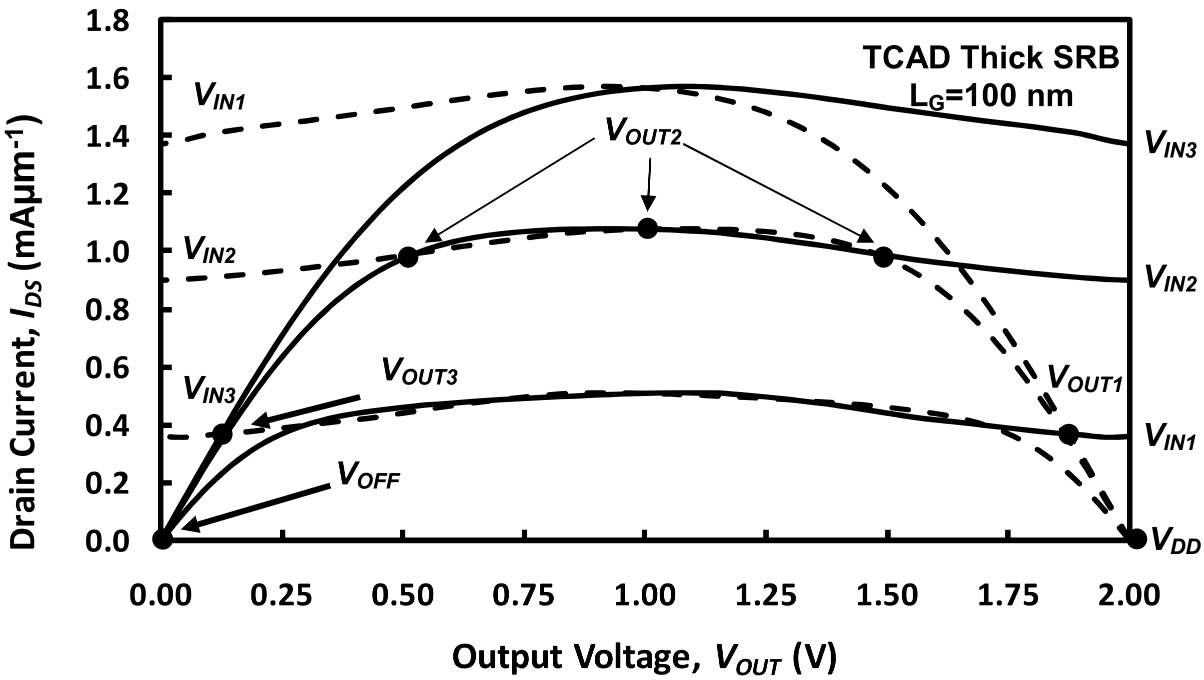

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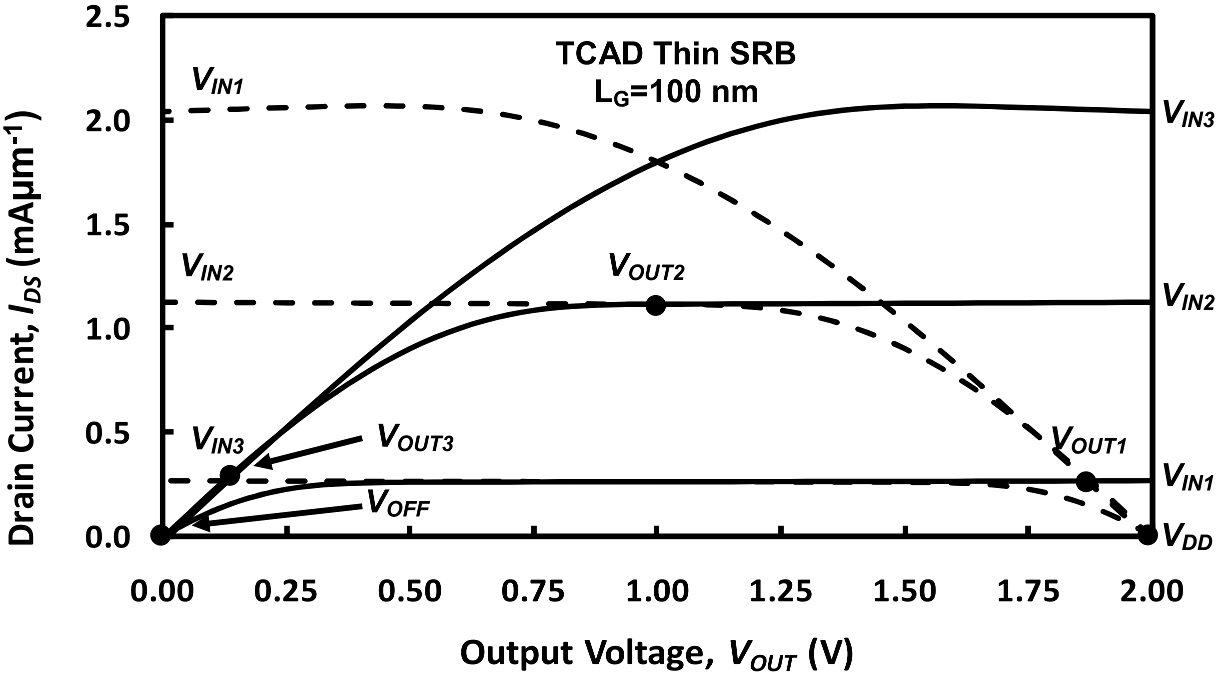

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